Development and creation of the method of information retrieval and recording electronics for 2D position-sensitive neutron detector

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The information retrieval from the delay line, consisting of 200 channels, was developed, and the recording electronics of the prototype 2D detector were also developed. The recording electronics connected to the cathode strips of the delay line contains signal preamps, time-to-code converters (TDC), amplitude-to-code converters (ADC), and a computer with a PCI interface card.

In this particle detection detector implemented cathodic method of information retrieval.

The location of the detected particle is determined by measuring four time intervals formed by a common start signal and stop signals taken from ends of the delay lines.

To collect information from the detector, a four-channel time-code converter (TDC) was developed; its general block diagram is shown in Fig.1

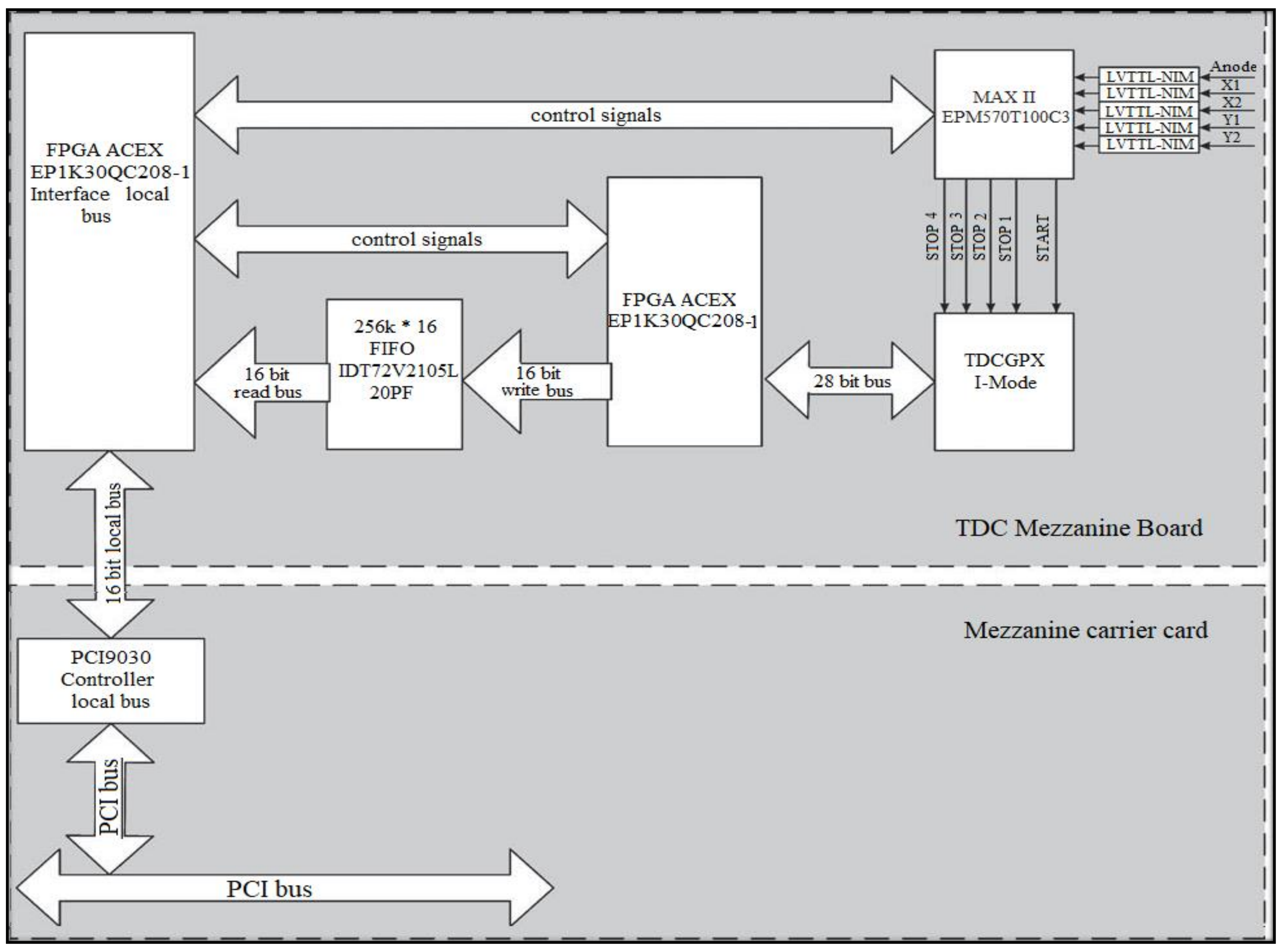

Fig. 1 General block diagram of the converter.

A delay line model was developed, composed of LC circuits with the parameters presented below on figure 2. The name of the coil and capacitor is LQH31HNR29J03L and GRM21A5C2E270JW01D.

- N = 200-number of chains
- inductance of one coil L = 290 nH; total inductance L_t = 290 * 200 nH
- capacitance of one capacitor C = 27 pF, total capacitance C_t = 27 * 200 pF
- wave impedance $Z_0 = \sqrt{(L / C)} \sim 100$ Ohm
- delay between taps $t_d = \sqrt{(LC)} = 2.8$ ns
- total delay time between N = 200 taps $T_{td} = n\sqrt{(LC)} = 560$ ns

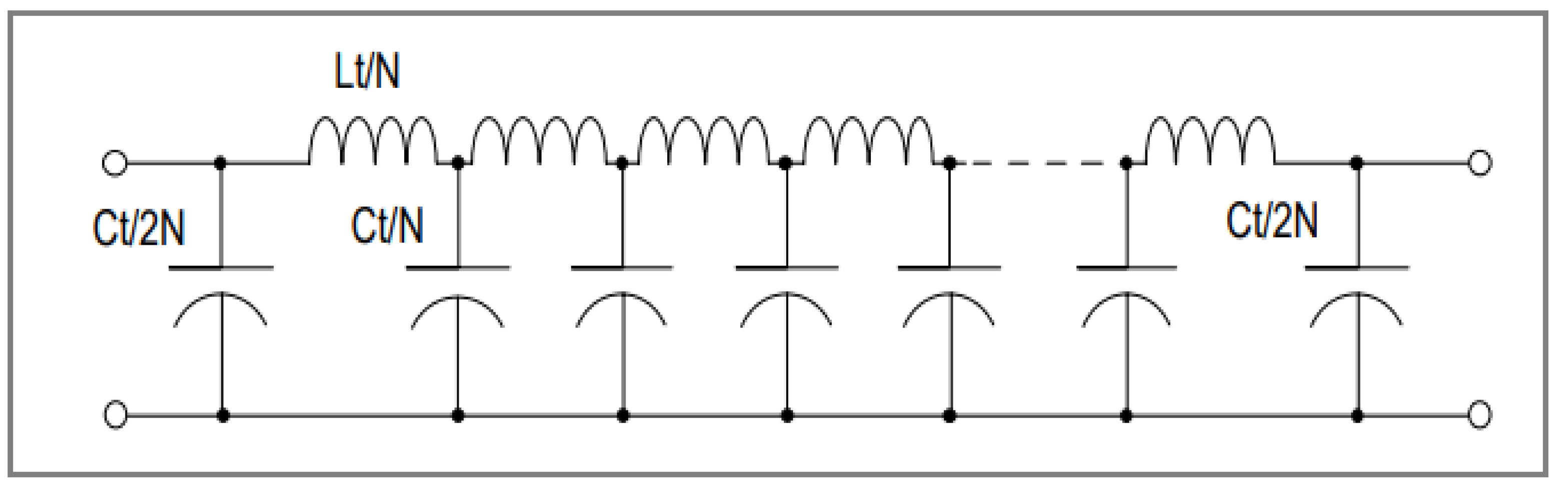

Fig. 2 Delay line circuit consisting of N number of LC circuits.

The simulation results of the delay line layout in the PSPICE software package are presented in the figure 3.

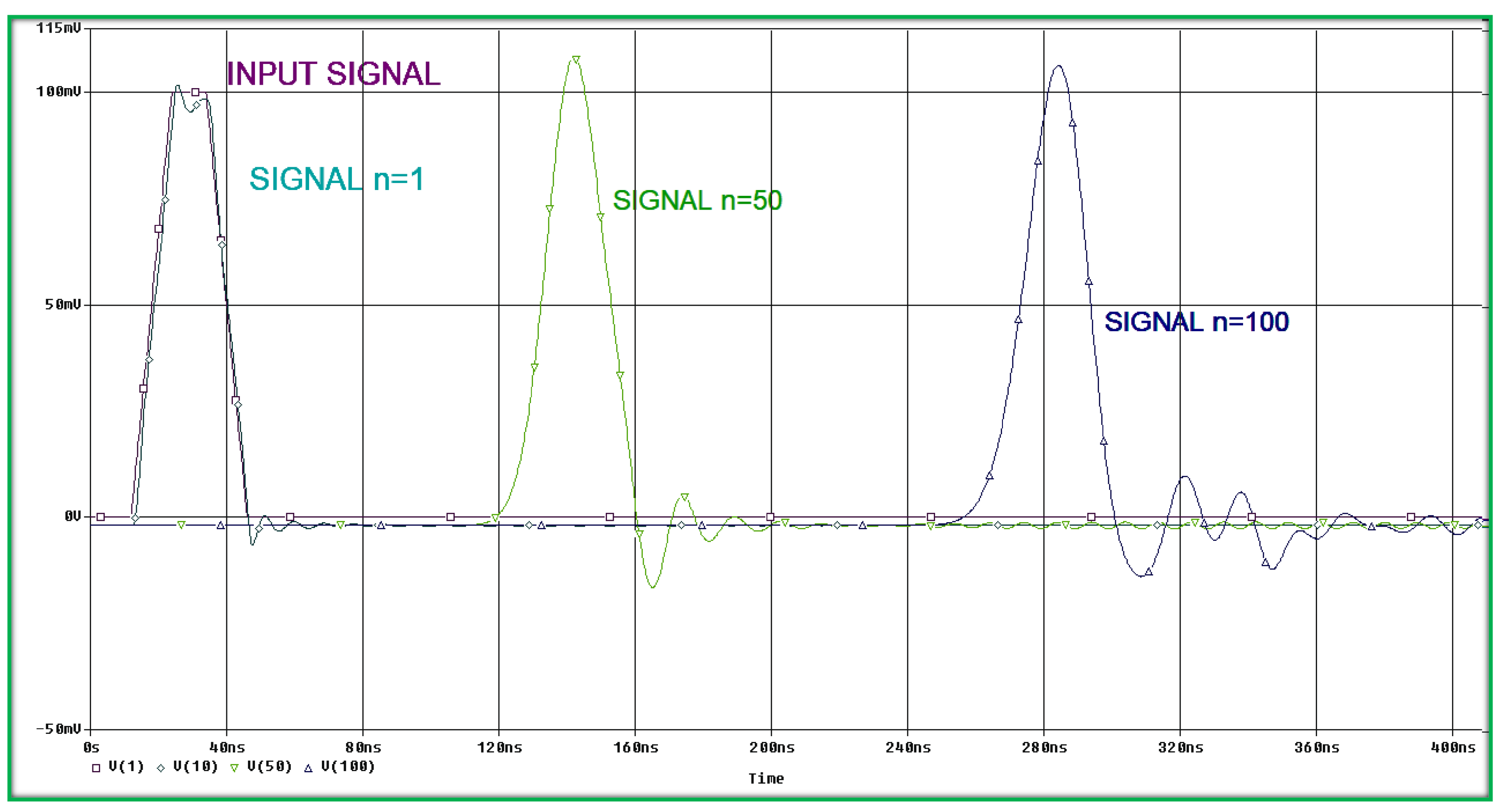

Fig. 3 Signal from the tap of the delay line N = 1, N = 50, N = 100

Communication with the PCI bus is carried out using the interface chip PCI 9030 manufactured by PLX Technology. TDC occurs using 16-pin local bus via two 40-pin female connectors.

The basis of the developed TDC is an eight-channel TD-CGPX converter chip used in I-MODE mode.

Programmable EPM570T100C3 adapted to receive conditions input signals randomly distributed over time. As a result of the measurement, four 16-bit words are formed, in each of which the three most significant bits determine the number of the conversion channel, and the remaining thirteen bits determine the data. The least significant bit of data is not used. Logic of signal and data exchange between TDCGPX time-code converter, FIFO memory and PCI 9030 interface microcircuit carried out by a programmable state machine implemented on two programmable logic matrices EP1K30QC208-1.

In the operating mode, the following main functions are implemented in the measurement process using software: data set when controlling the filling of the buffer FIFO-memory, reading the memory after half-filling it, processing and storing data. When the FIFO memory overflow sign appears, the data set is stopped and read. If a hardware stop signal is detected or goes beyond the set time window, the event is considered false.

Software hardware complex characteristics:

- the delay time of the distributed coordinate lines of the detector is < 600 ns;
- the number of channels for converting time intervals into a digital code is 4;;
- differential non-linearity of conversion scales at sensitivity 162 ps / channel <5%;
- the time of measuring and recording the event in the FIFO buffer memory <2 μs;
- System throughput > 150,000 events per second.

Figure 4 shows a screenshot of the software, which shows the 4 time intervals used to determine the location of the particle.

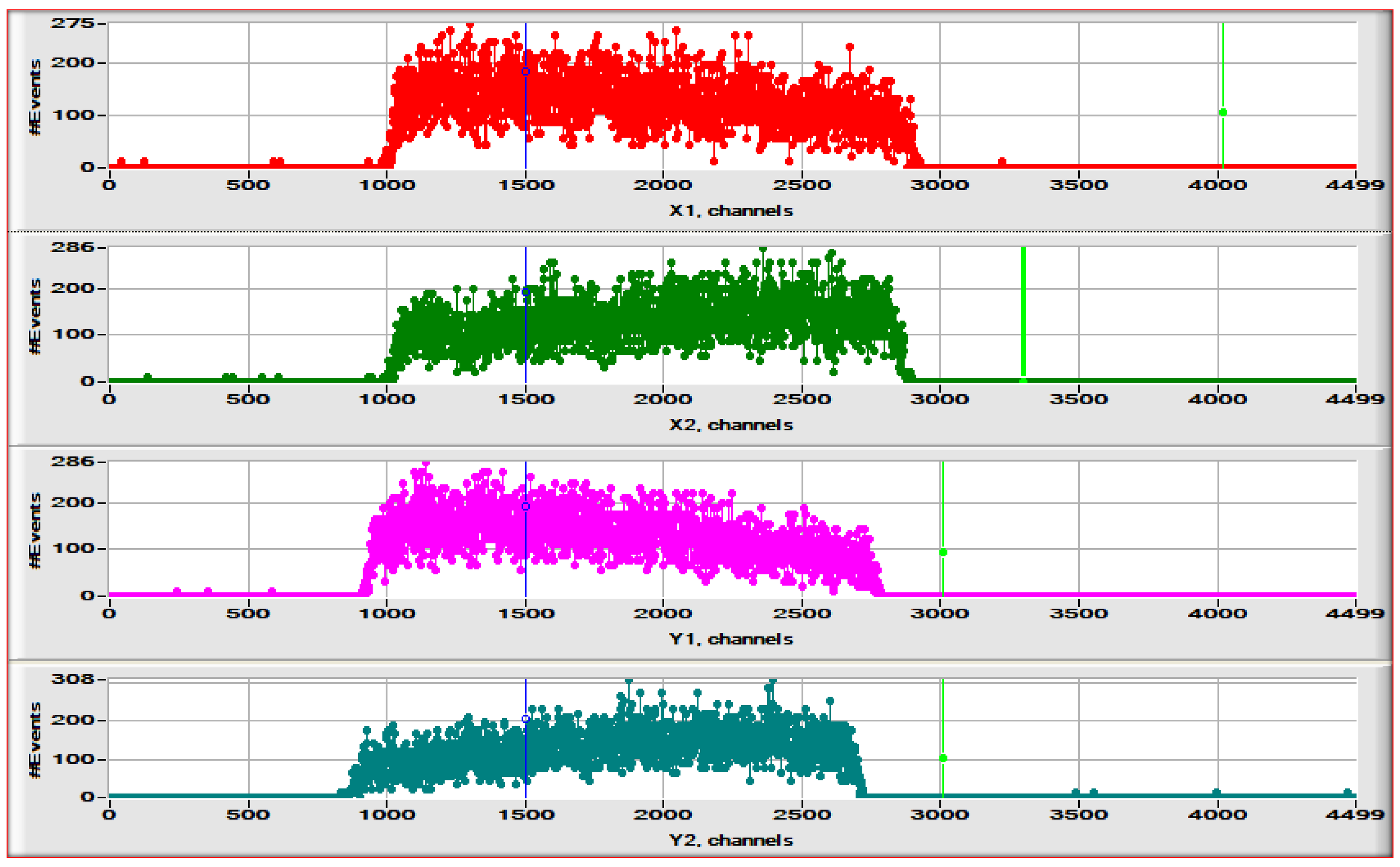

Fig. 4 time intervals X1, X2, Y1, Y2

Figure 5 shows a screenshot of the detector software illustrating the operation of the developed electronics kit.

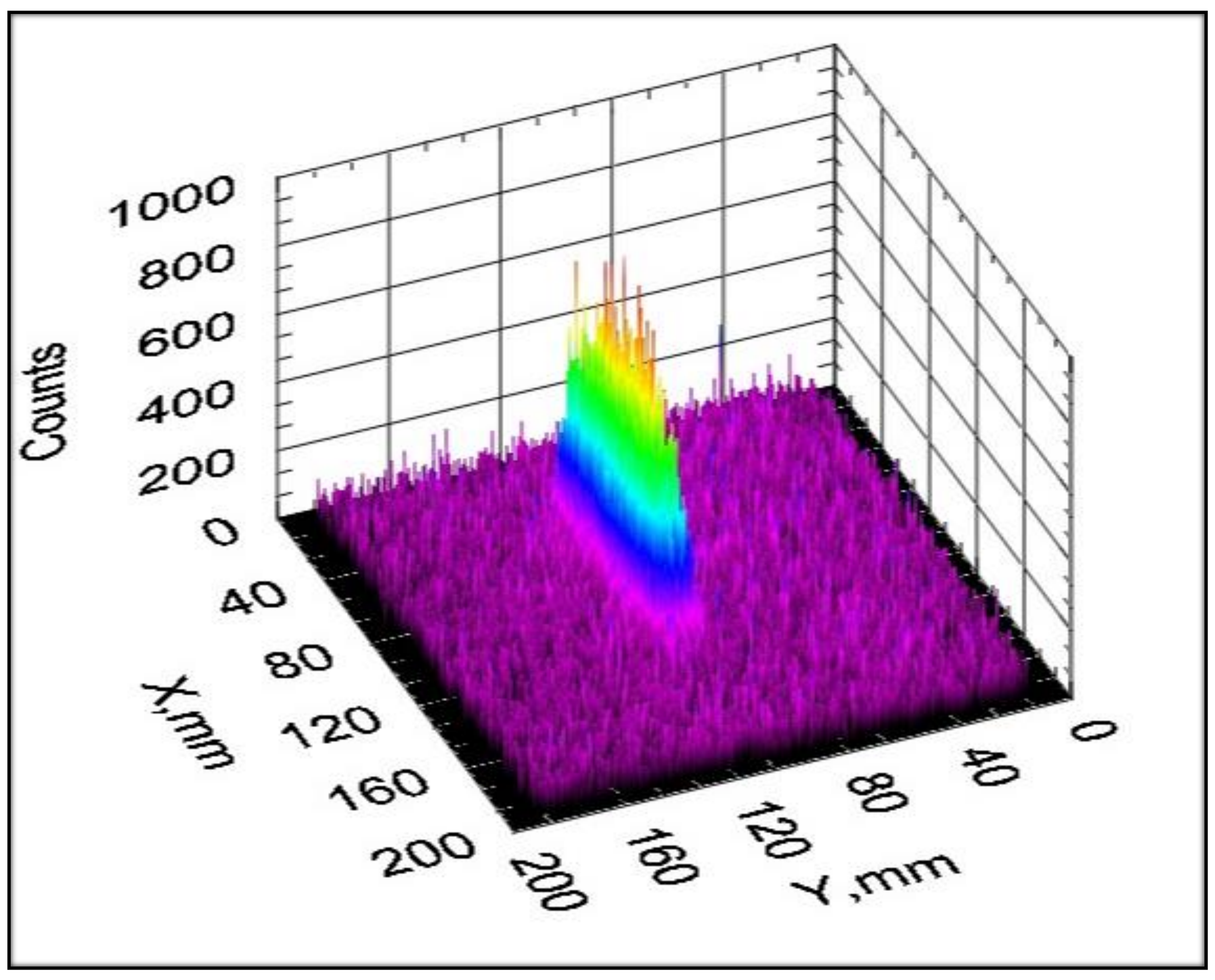

Fig. 5 spectrogram of a neutron beam passing through a limiting slit

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